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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/417,980	10/13/1999	LINUS TORVALDS	TRANS12	8220

7590 06/24/2004

Wagner Murabito & Hao LLP
Two North Market Street
Third Floor
San Jose, CA 95113

EXAMINER	
ELLIS, RICHARD L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/417,980	TORVALDS ET AL.	
	Examiner	Art Unit	
	Richard Ellis	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8* is/are allowed.

6)☒ Claim(s) *1,4,5 and 7* is/are rejected.

7)☒ Claim(s) *2 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 October 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-2 and 4 remain for examination. Claims 5-8 are newly presented for examination.

2. The drawings are objected to under 37 CFR § 1.83(a). The drawings must show every feature of the invention specified in the claims. The provided drawings consist of four figures showing execution paths through example code sequences. There are no flowcharts corresponding to any of the method steps recited in any of claims 1-2 and 4-8. Additionally, all hardware elements recited by any of claims 1-2 and 4-8 are also missing from the drawings. Therefore both the method steps of all the claims, plus all hardware elements and their interconnection which are recited by all the claims must be shown or the features canceled from the claim. No new matter should be entered.

3. Applicant is required to submit a proposed drawing correction in response to this Office Action. Any proposal by the applicant for amendment of the drawings to cure defects must consist of two parts:

a) A *separate* letter to the Draftsman in accordance with MPEP § 608.02(r); and,

b) A print or pen-and-ink sketch showing changes in *red ink* in accordance with MPEP § 608.02(v).

4. The following in a quotation of the first paragraph of 35 USC 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. New claim 7 is rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In the specification, applicant's provide two alternate definitions for the term "speculating". The first definition, given on pg. 2 lines 12-22, is that of storing effects of instruction execution in temporary memory until execution completes successfully. The second definition, given on pg. 8, lines 10-22, is that of translation and optimization software guessing that a branch will likely be taken and not inserting a commit point in order to accelerate execution. These are the only two definitions provided by

applicant's in their specification for the term "speculating". However, applicant's claim 7 uses the term "speculating" in the context of execution of instructions ("a method of executing instructions in a host microprocessor ...") wherein the method comprises "speculating that execution of a branch instruction will cause a branch ...". Since this claim is using speculating in terms of a branch, it is clear that it should refer to applicant's second definition on pg. 8 of the specification. However, applicant's definition on pg. 8 of the specification relates the term speculating to the translation and optimization software, and makes absolutely no mention of what operations any host processor will perform as a consequence of that branch. At no point in applicant's specification does it ever indicate that the processor, when executing instructions, will speculate that a branch is taken. The only speculation in the specification is that related to the translation software's decision to include or not to include a commit point as part of the translated instruction stream. Since this translation occurs prior to execution by the processor, it gives no indication that the host processor has any capability to perform the same speculation, and therefore, it appears that applicant's did not in fact have possession of the invention now claimed in claim 7.

6. Claim 7 is rejected under 35 USC 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. For the same reasons detailed above in regards to claim 7, applicant's specification does not enable a processor to perform speculation that a branch will be taken because the specification makes absolutely no mention of what operations a processor will perform as a result of the branch. Accordingly, the disclosure does not enable one of ordinary skill in the art to make and/or use the invention now claimed in claim 7.

7. Claims 5-6 rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7.1. The scope of meaning of the following terms are unclear:

7.1.1. "from a target instruction set a target processor to sequences" claim 5; This clause is

grammatically incorrect and appears to be missing one or more words.

8. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a)shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1 and 4 are rejected under 35 USC § 102(b) as being clearly anticipated by Robinson et al., U.S. Patent 5,307,504.

11. Claims 1 and 4 are rejected under 35 USC § 102(e) as being clearly anticipated by Kelly et al., U.S. Patent 5,958,061.

Robinson et al. and Kelly et al. were cited as prior art references in paper number 6, mailed February 12, 2004.

12. The rejections are respectfully maintained and incorporated by reference as set forth in the last office action, paper number 6, mailed February 12, 2004.

13. New Claim 5 is rejected under 35 USC 102(b) as being clearly anticipated by Robinson et al., U.S. Patent 5,307,504.

Robinson et al. taught (e.g. see figs. 1-5b) the invention as claimed (as per new claim 5), including a data processing ("DP") system comprising:

13.1. a method for use by a host microprocessor (col. 4 lines 40-44) which translates sequences of instructions (col. 4 lines 35-36, additionally, the flowchart of figure 3 shows that plural X instructions are translated by the method disclosed by Robinson et al., see box 74, labeled "MORE X INSTRUCTIONS") from a target instruction set a target processor (col. 4 lines 38-40) to sequences of instructions for the host microprocessor (col. 4 lines 35-38) comprising the steps of:

(note, that because Robinson et al. is translating plural X instructions into Y instructions (see fig. 3, box 74), a system incorporating Robinson et al.'s invention will inherently have plural sets of figure 6 present in it's output, one each of G1 through G4 for each input X instruction. For convenience in rejecting the following claim language, applicant's attention is drawn to attachment A, which is an annotated duplicate of Robinson et al.'s figure 6, duplicated three times, to show how applicant's claim language remains anticipated by Robinson et al.)

13.2. beginning execution of a first sequence of target instructions (I21) by committing state of the target processor and storing memory stores generated by previously executed sequences of instructions at a point in execution of instructions at which state of the target processor is known (I12, state of the processor is known at I12);

13.3. executing a sequence of host instructions (I21) from the first sequence of target instructions commencing immediately after committing state of the target processor (I21 occurs immediately after I12) and storing memory stores previously generated by execution until another point in the translation of target instructions at which state of the target processor is known (I22, state of the processor is again known at I22, which is "another" point where state is known);

13.4. beginning execution of a next sequence of target instructions (I31, which is after I21, therefore a "next" sequence) by committing state of the target processor and storing memory stores generated by the execution of the first sequence of target instructions at the another point (I22, which is the point where state is known, and is where state is saved in preparation for I31) in the translation of target instructions at which state of the target processor is known; and,

13.5. executing a sequence of host instructions from the next sequence (I31) of target instructions commencing immediately after committing state of the target processor (I31 occurs immediately after I22) and storing memory stores generated by execution of the

first sequence of target instructions until a further point (I32) in the translation of target instructions at which state of the target processor is known (state is known at I32, and I32 is a further point because it is after I22 and I31).

14. New claim 5 is rejected under 35 USC 102(e) as being clearly anticipated by Kelly et al., U.S. Patent 5,958,061.

In a manner similar to the analysis of claim 5 in view of Robinson et al. above, Kelly et al. will inherently have a sequence of instructions and context save points because the disclosed system is operating on more than one single instruction (col. 9 lines 25-32, note "running instructions of a different" where "instructions" is plural). Correspondingly, in exactly the same manner as detailed for Robinson et al., Kelly et al.'s system will always have a context save point immediately prior to a stream of instructions that are executed, and as well, another context save point after the stream of instructions is finished. Therefore, Kelly et al. also anticipates new claim 5.

15. New claim 7 is rejected under 35 USC 102(b) as being clearly anticipated by Robinson et al., U.S. Patent 5,307,504 and Sites, U.S. Patent 5,428,786.

The elements of claim 7 which are in common with claims 1 and 4-5 are rejected over Robinson et al. for the same reasons presented elsewhere. Additionally, it is noted that figure 6 of Robinson et al. shows that a granule, consisting of elements G1 through G4 exists for each X instruction. Therefore, for each instruction, including branch instructions, there will exist a G3 and G4 portion of a granule. Therefore, as to the second clause of the claim, a branch instruction (fig. 6, X_0) will consist of a G1 through G4 element, and therefore, each branch will commit state (G3, G4) after the branch is executed (G1, G2) and prior to beginning a next instruction (a next G1 of a next granule of a next X instruction). Furthermore, although the text of the Robinson et al. disclosure does not itself mention speculating upon the outcome of a branch, Sites taught speculating upon the outcome of a branch for translation purposes (col. 29 lines 55-62). The Sites patent is incorporated by reference into the disclosure of Robinson et al. at col. 1 lines 26-28. Accordingly, Robinson et al. did in fact teach exactly the type of "speculation" as defined in applicant's specification at page 8.

16. New claim 7 is rejected under 35 USC 102(e) as being clearly anticipated by Kelly et al., U.S. Patent 5,958,061.

The statements regarding the Kelly et al. reference and rejections based upon the Kelly et al. reference are incorporated herein by reference. As to the newly claimed speculation aspect of the claim, Kelly et al. also taught speculative execution (col. 13 lines 48-58) and therefore anticipates the claim.

17. Applicant's arguments filed May 6, 2004 have been fully considered but they are not deemed to be persuasive.

18. In the remarks, applicant argues in substance:

18.1. That: "Robinson fails to teach or suggest that state is immediately committed at the beginning of a speculative sequence of host instructions. Applicants assert that even if the G3 and G4 instructions taught by Robinson are interpreted as committing state, these instructions follow the G1 and G2 instructions. Thus, the G3 and G4 instructions are always the last instructions in the sequence of "y" instructions. Hence, Applicants respectfully assert that Robinson does not teach or suggest the claimed limitation of 'beginning execution of a speculative sequence of host instructions following a branch from the first sequence of target instructions by immediately committing state and storing memory stores.'".

This is not found persuasive because applicant has both mis-quoted and addressed only a portion of the claim language, and by doing such has inserted a limitation which does not exist in the claims and omitted an important claim limitation which immediately follows the quoted claim language. The complete, accurate, language of this claim clause is as follows:

> "beginning execution of a first sequence of target instructions by committing state of the target processor and storing memory stores generated by previously-executed sequences of instructions at a point in the execution of instructions at which state of the target processor is known"

It is noted that the claim text as presented by applicant does not contain the limitation "immediately committing state ..." but merely "committing state". It is also noted that the claim states that the committing state occurs "**at a point in the execution of instructions at which state of the target processor is known**". This is the only claim limitation which places any timing limitation upon when within the method the "committing state" step occurs, and the limitation of timing that the language states is that it occurs "at a point ... at which state ... is known". In the case of Robinson et al., the G3 and G4 instructions are located "at a point ...

at which state ... is known" and they commit state of the target processor in preparation for "beginning execution of a first sequence" (a sequence which follows the G3 and G4 instructions). Accordingly, Robinson et al. "begins execution of a sequence of instructions (G1, G2) by storing state (G3, G4) at a point in the execution of instructions at which state of the target processor is known (at the completion of a previous granule).

18.2. That: "Claim 1 further recites, 'a speculative sequence of host instructions following a branch.' The rejection states that Applicants' specification defines a possible meaning of speculation as, 'the temporary storage of results until execution has completed successfully.' Applicants do not deny that the definition of speculation may encompass, "the temporary storage of results until execution has completed successfully.' Applicants assert, however, that the definition of speculation is not limited to, "the temporary storage of results until execution has completed successfully.'"

This is not found persuasive because applicant's have admitted that one accepted meaning, as set forth in their specification, for "speculation" is that of "the temporary storage of results until execution has completed." Applicant's suggestion of a second alternative definition for "speculation" is noted. Applicant's claim language, however, provides no guidance as to which of the alternative definitions for "speculation" the claims are to be limited to, and therefore, applicant's claims are so broad as to encompass both definitions. Accordingly, because Robinson et al. teaches at least one definition for "speculation" and applicant's claims to not limit the scope of the invention to exclude that definition taught by Robinson et al., then Robinson et al. in fact does read upon applicant's claims. In order to overcome Robinson et al. with applicant's suggested alternative definition, applicant's must amend the claim language to clearly specify, within the claim language itself, that the desired definition for "speculation" is limited only to applicant's alternative definition. This argument also applies to claim 4.

18.3. Applicant's arguments regarding the Babaian et al. reference are convincing. Babaian et al. does not have support for the material disclosed in the publication within the provisional parent applications. Accordingly, the Babaian et al. publication does not have an effective filing date prior to applicant's effective filing date. Therefore, the rejection over Babaian et al. has been withdrawn.

18.4. That: "Kelly fails to teach or suggest, "beginning execution of a speculative sequence of host instructions following a branch from the first sequence of target instructions by immediately committing state and storing memory stores," as claimed. ...

This is not found persuasive for the same reasons as discussed with regards to Robinson et al. and claim 1, supra. Applicant's claims only limit the location of the commitment to that when "state is known". As such, by committing after a sequence, as admitted by applicant, Kelly et al. is storing state at a point in execution where the state is known, and in preparation for beginning a next sequence of instructions. This argument also applies to claim 4.

18.5. That: "Applicants respectfully assert that the prior art fails to teach or suggest, "executing a sequence of host instructions from the first sequence of target instructions commencing immediately after committing state of the target processor and storing memory stores previously generated by execution" [as per new claim 5]."

This is not found persuasive because as seen in the rejection of new claim 5, supra., Robinson et al. does teach executing a sequence of host instructions (I21) immediately after committing state (I12).

19. Claims 2 and 6 are objected to as being dependent upon a rejected base claim, but would render the base claim allowable if bodily incorporated into the base claim such that the new base claim included all of the original limitations of the base claim, any intervening claims, and the objected claim.

20. Claim 8 is allowable over the prior art of record.

21. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

22. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (703) 305-9690. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712. The fax phone number for the USPTO is: (703)872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

RICHARD L. ELLIS
PRIMARY EXAMINER

Richard Ellis
June 22, 2004

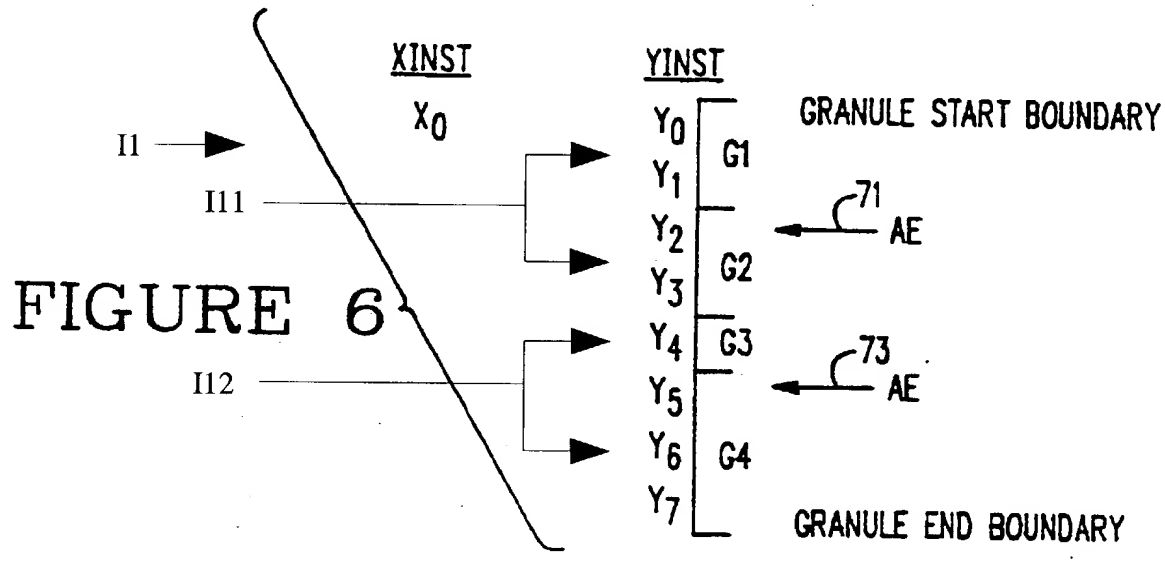

FIGURE 6

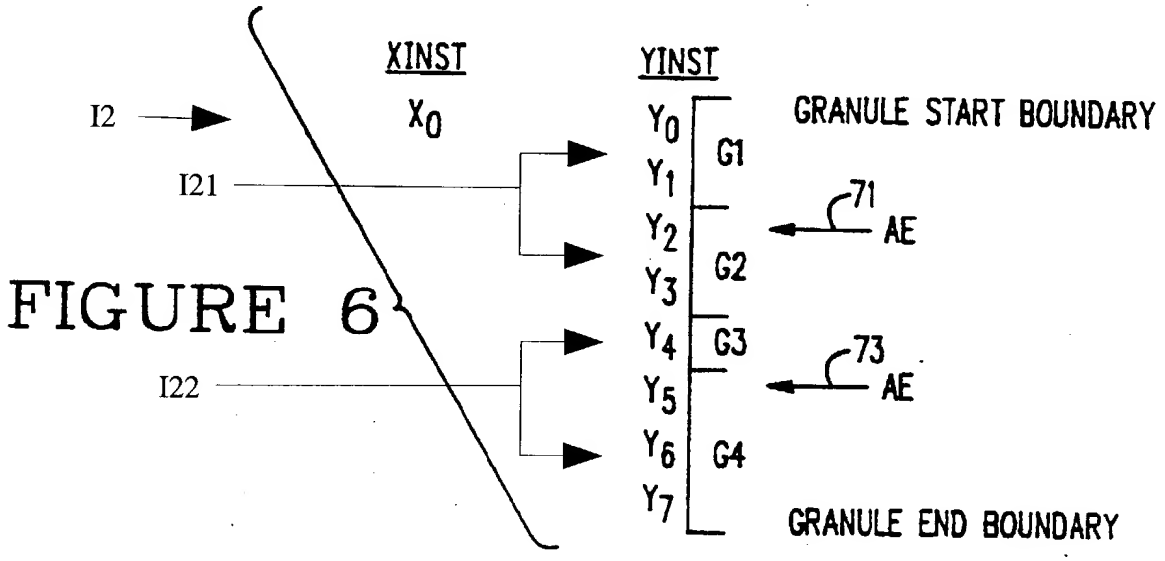

FIGURE 6

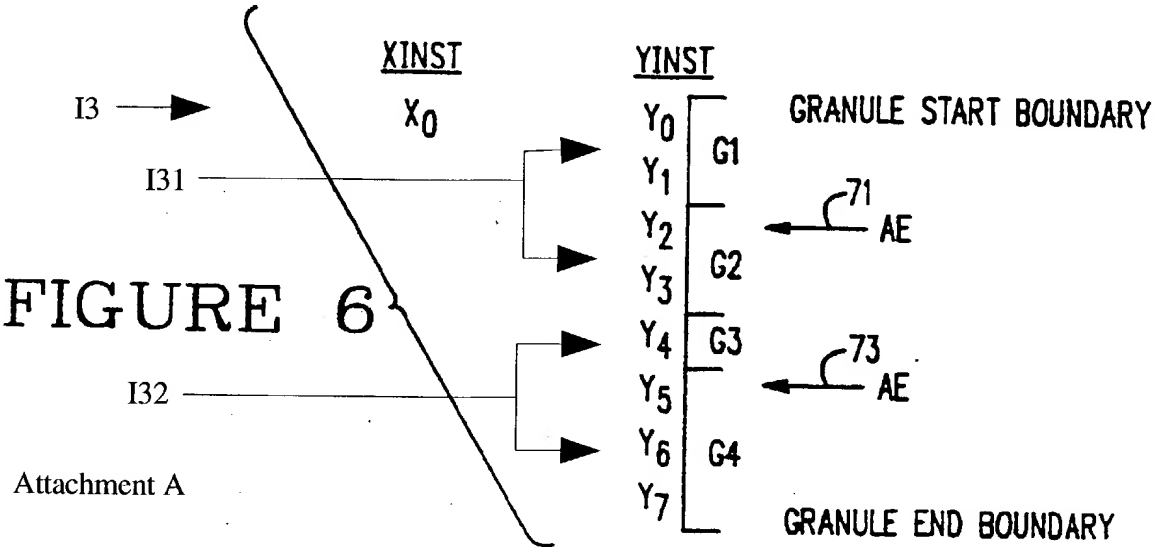

FIGURE 6

Attachment A